Title: CACHE INTEGRITY APPARATUS, SYSTEMS, AND METHODS

Assignee: Intel Corporation

REMARKS

This communication responds to the Office Action mailed on August 4, 2005. Claims 10, 16, 19, and 23 are amended, no claims are canceled, and no claims are added. As a result, claims 1-23 are now pending in this Application. It is respectfully noted that claim 10 has been amended to correct a typographical error, and not for reasons related to patentability.

Submission of Formal Drawings

Two sheets of formal drawings are submitted herewith, each identified as "REPLACEMENT SHEET." It is believed that the drawings are in compliance with 37 CFR 1.84. No amendments have been made to the drawings.

Objections to the Specification

The Office has objected to the title of the application as not being descriptive. The title has been changed to a more descriptive form, so as to address the concerns expressed by the Office. The Office has also objected to the Abstract as not being adequately descriptive of the subject matter of the invention. The abstract has been amended to describe a particular embodiment, rendering the objection moot. Finally, the office has objected to the specification due to informalities, namely, a typographical error. It is believed that the amendment made herein to the specification obviates said objection, and renders it moot. The Applicant appreciates the Examiner's thorough review in this regard.

§112 Rejection of the Claims

Claim 21 was rejected under 35 USC § 112, first paragraph, as failing to comply with the enablement requirement. In particular, it is asserted that "the claimed 'device option memory' is unclear." The Applicant respectfully disagrees.

A device option memory is well-known to those of ordinary skill in the art, including, for example, such items as an option read only memory (OROM or OPROM),

Filing Date: June 27, 2003

Title: CACHE INTEGRITY APPARATUS, SYSTEMS, AND METHODS

Assignee: Intel Corporation

which may comprise "... firmware that is called by the system BIOS. For example, an adapter card that controls a boot device might contain firmware that is used to connect the device to the system once the Option ROM is loaded." See http://en.wikipedia.org/wiki/Option ROM.

M.P.E.P. § 2164 et seq. notes that the burden is on the Examiner to establish a prima facie case to maintain a rejection of non-enablement with respect to the disclosure of a patent application under 35 U.S.C. § 112, first paragraph. Such a case requires:

- 1. a rational basis as to
 - a. why the disclosure does not teach, or
 - b. why to doubt the objective truth of the statements in the disclosure that purport to teach;
- 2. the manner and process of making and using the invention;
- 3. that correspond in scope to the claimed invention;
- 4. to one of ordinary skill in the pertinent technology;
- 5. without undue experimentation; and
- 6. dealing with subject matter that would not already be known to the skilled person as of the filing date of the application.

"The Examiner must provide evidence ... supporting each of these elements for a rejection under the first paragraph of § 112 to be proper." See Patent Prosecution, Practice and Procedure Before The United States Patent Office, Ira H. Donner, pg. 691, 2002.

Since evidence supporting each of the required elements noted above (e.g., that one of ordinary skill would be unable to practice embodiments of the invention without undue experimentation) has not been presented, a prima facie case for non-compliance under § 112, first paragraph, has not been established with respect to claim 21. Reconsideration and withdrawal are respectfully requested.

Claims 1-23 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Since a prima facie case of indefiniteness has not been established, the Applicant respectfully traverses this rejection.

Serial Number: 10/607,772 Filing Date: June 27, 2003

Title: CACHE INTEGRITY APPARATUS, SYSTEMS, AND METHODS

Assignee: Intel Corporation

It is noted that "[in] relation to Section 112, second paragraph, the Examiner has the burden of showing that the proposed claim language is indefinite to one of skill in the art." See Patent Prosecution: Practice and Procedure Before the U.S. Patent Office by Irah H. Donner, pg. 831, 2002. To make out a *prima facie* case of indefiniteness, three elements must be shown:

- 1) interpretation of the claim in light of the specification;
- 2) interpretation of the claim as one of ordinary skill in the art would interpret it; and
- 3) that the limitations in the claim, or the subject matter not in the claim, does not reasonably define the invention.

Title: CACHE INTEGRITY APPARATUS, SYSTEMS, AND METHODS

Assignee: Intel Corporation

It is respectfully noted that "[a]n Examiner must clearly define the problem and why it is a problem in connection with the issue of claim definiteness in order to provide an applicant or any reviewing authority with the information necessary to evaluate the Examiner's position fairly." *Id.* at pg. 832.

Nothing has been stated by the Office respecting the claim language in relation to how it would be interpreted by one of skill in the art (e.g., why one of ordinary skill in the art would have any difficulty implementing a "memory cached by a non-volatile cache" or an "operating system cache driver"). In fact, such terminology is commonly used in industry.

For example, at the Microsoft® developer network web site, in a description of the Microsoft® Windows® NdisMAllocateSharedMemory function, it is noted that if "the allocated memory is cached and, therefore, needs to be flushed on transfers, the miniport must call NdisAllocateBuffer to allocate an NDIS_BUFFER type descriptor for the shared memory range." See

http://msdn.microsoft.com/library/default.asp?url=/library/en-

us/wceddk40/html/cxrefndismallocatesharedmemory.asp. (emphasis added) Another example includes information provided with respect to an operating system cache driver called Vcache, which is "the **Windows 32-bit protected-mode cache driver** ... [that] determines the maximum cache size based on the amount of RAM that is present when Windows starts." See http://support.microsoft.com/kb/q253912/. (emphasis added)

Since a *prima facie* case of indefiniteness has therefore not been established, it is respectfully requested that this rejection of claims 1-23 under 35 USC § 112, second paragraph, be reconsidered and withdrawn.

With respect to the rejection of claims 14, 16, 19, and 23 under 35 USC § 112, second paragraph, it is respectfully noted that claim 14 recites "a memory to store an address" and "a memory cached by the non-volatile cache". Claims 16, 19, and 23 have thus been amended to clarify that the "memory" recited therein refers to the "memory to store an address." This amendment was therefore not made for reasons related to patentability. The Applicant apologizes for any confusion in this regard, and respectfully

Title: CACHE INTEGRITY APPARATUS, SYSTEMS, AND METHODS

Assignee: Intel Corporation

request reconsideration and withdrawal of this rejection of claims 14, 16, 19, and 23 under 35 USC § 112, second paragraph.

§103 Rejection of the Claims

Claims 1-4, 6-10, 14, 16 and 19 were rejected under 35 USC § 103(a) as being unpatentable over Sarkozy et al. (U.S. 5,732,238; hereinafter "Sarkozy") in view of Handy (The Cache Memory Book, Academic Press, 1998; hereinafter "Handy"). Claims 5, 17, 18 and 20 were rejected under 35 USC § 103(a) as being unpatentable over Sarkozy in view of Handy and further in view of Lee et al. (U.S. 5,937,433; hereinafter "Lee"). Claims 11 and 23 were rejected under 35 USC § 103(a) as being unpatentable over Sarkozy in view of Handy and further in view of Howard (U.S. 6,629,198; hereinafter "Howard"). Claim 12 was rejected under 35 USC § 103(a) as being unpatentable over Sarkozy in view of Handy and further in view of Heemels (U.S. 5,603,331; hereinafter "Heemels"). Claim 15 was rejected under 35 USC § 103(a) as being unpatentable over Sarkozy in view of Handy and further in view of Kozierok (hereinafter "PC Guide"). Claim 22 was rejected under 35 USC § 103(a) as being unpatentable over Sarkozy in view of Handy and Lee, and further in view of PC Guide. First, the Applicant does not admit that Sarkozy, Handy, Lee, Howard, Heemels, or PC Guide are prior art and reserves the right to swear behind these references in the future. Second, since a prima facie case of obviousness has not been established as required by M.P.E.P. § 2142, the Applicant respectfully traverses these rejections.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.* The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge

'Serial Number: 10/607,772 Filing Date: June 27, 2003

Title: CACHE INTEGRITY APPARATUS, SYSTEMS, AND METHODS

Assignee: Intel Corporation

generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicants disclosure. *M.P.E.P.* 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference. *In re Oetiker*, 977 F.2d 1443, 24 U.S.P.Q.2d (BNA) 1443 (Fed. Cir. 1992). However, while it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 U.S.P.Q.2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 U.S.P.Q. 171, 174 (C.C.P.A. 1979)). The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which notes that the motivation must be supported by evidence in the record.

No proper *prima facie* case of obviousness has been established because (1) combining the references does not teach all of the limitations set forth in the claims, (2) there is no motivation to combine the references, and (3) combining the references provides no reasonable expectation of success. Each of these points will be explained in detail, as follows.

Combining The References Does Not Teach All Claim Limitations.

First, with respect to independent claims 1, 9, 14, and 19, it is admitted in the Office Action that Sarkozy does not disclose "that recording an address of a write operation should be done prior to executing an operating system driver." The Office goes on to assert that "Handy explains that disk caches are often implemented in dynamic RAM using software control." However, this fact alone does not imply any particular

Serial Number: 10/607,772 Filing Date: June 27, 2003

Title: CACHE INTEGRITY APPARATUS, SYSTEMS, AND METHODS

Assignee: Intel Corporation

actions with respect to the sequencing of disk cache control operations. In fact, the Applicant's representative was unable to find anything within the bounds of Handy to support recording write operation addresses prior to "executing an operating system cache driver" or "booting an operating system cache driver," as claimed in independent claims 1, 9, 14, and 19. Lee, Howard, Heemels, and PC Guide also fail in this respect.

Therefore, no combination of Sarkozy, Handy, Lee, Howard, Heemels, or PC Guide can provide recording write operation addresses prior to "executing an operating system cache driver" or "booting an operating system cache driver," as claimed by the Applicant in independent claims 1, 9, 14, and 19, and a *prima facie* case of obviousness has not been established. Further, it is respectfully noted that if an independent claim is nonobvious under 35 USC § 103, then any claim depending therefrom is also nonobvious. *See* M.P.E.P. § 2143.03. Therefore, claims 2-8, 10-13, 15-18, and 20-23 are also nonobvious.

There Is No Motivation to Combine the References.

Handy's express concern with cache operational speed (e.g., "This book pertains only to CPU caches and not to disk caches. ... CPU caches operate at such high speed that hardware control must be used, and the cache itself must be implemented in static RAM.) teaches away from using the non-volatile cache technology of Sarkozy. *See* Handy, pg. xv. Adding any one or more of Lee, Howard, Heemels, and PC Guide does nothing to negate the teaching of Handy.

References must be considered in their entirety, including parts that teach away from the claims. See MPEP § 2141.02. The fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. In this case, Handy teaches that such a combination would *not* be desirable.

Combining the References Provides No Reasonable Expectation of Success.

Implementing a disk cache "in dynamic RAM (DRAM) using software control" as taught by Handy does nothing to promote recording write operation addresses prior to "executing an operating system cache driver" or "booting an operating system cache

Serial Number: 10/607,772 Filing Date: June 27, 2003

Title: CACHE INTEGRITY APPARATUS, SYSTEMS, AND METHODS

Assignee: Intel Corporation

driver," as claimed by the Applicant. Since the Office admits this element is missing from Sarkovy, no reasonable expectation of successfully modifying Sarkovy to provide this order of operation can be entertained. Lee, Howard, Heemels, and PC Guide also fail to add anything to this combination that leads to the reasonable expectation of success.

In summary, none of the references teach recording write operation addresses prior to "executing an operating system cache driver," as set forth in independent claims 1, 9, 14, and 19. No evidence has been entered in the record to support a need to combine the references (in fact the references teach away from the proposed combinations), and no reasonable expectation of success results from any combination. The requirements of *M.P.E.P.* § 2142 have not been satisfied, and a *prima facie* case of obviousness has not been established with respect to these independent claims. All dependent claims are also nonobvious, since claims depending from nonobvious independent claims are also nonobvious. It is therefore respectfully requested that the rejections to claims 1-12 and 13-23 under 35 U.S.C. § 103 be reconsidered and withdrawn.

Allowable Subject Matter

Claim 13 was not addressed in the Office Action, and the Applicant assumes that this claim is in condition for allowance. Claim 14 was indicated to be allowable if rewritten to overcome the rejection(s) under 35 USC § 112, second paragraph, set forth in the Office Action and to include all of the limitations of the base claim and any intervening claims. However, claim 14 was also rejected under 35 USC § 103(a). The Applicant has addressed the rejection of this claim under both headings, above, and believes claim 14 is also in condition for allowance.

Page 17 Dkt: 884.905US1 (INTEL)

Serial Number: 10/607,772 Filing Date: June 27, 2003

Title: CACHE INTEGRITY APPARATUS, SYSTEMS, AND METHODS

Assignee: Intel Corporation

CONCLUSION

The Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicant's attorney Mark Muller at (210) 308-5677, or the undersigned at (612) 349-9592 to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

ROBERT ROYER ET AL.

By their Representatives, SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. Attorneys for Intel Corporation P.O. Box 2938 Minneapolis, Minnesota 55402 (612) 349-9592

Date . 2005	By ann M. M. Cack	
	Ann M. McCrackin	
	Reg. No. 42,858	

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this _30th_ day of September 2005.

Anne M. Richards	anulh R
Name	Signature